

**SRI VIDYA COLLEGE OF ENGINEERING & TECHNOLOGY,
VIRUDHUNAGAR**



Department of Electrical & Electronics Engineering

Cordially invite you to the

**FACULTY DEVELOPMENT PROGRAM on
“DESIGN OF ELECTRICAL MACHINES”**

09th December, 2017

in the EEE Power System Simulation Lab

Er.R.THIRUVENGADA RAMANUJA DOSS B.E.,
Chairman, Sri Vidya group of Institutions, Virudhunagar.

&

Er.T.VENKATESH B.E.,
Vice Chairman, Sri Vidya group of Institutions, Virudhunagar.

Presides over the function

Mr.P.I.D.T.BALA DURAI KANNAN,
Assistant Professor & HoD / EEE Department,
Sri Vidya College of Engineering & Technology

Has kindly consented to be the guest and

Delivers the special address

In the presence of

Dr.S.SANKARALINGAM

Principal, Sri Vidya college of Engg. & Tech, Virudhunagar

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AGENDA

Date: 08.12.17

Time: 10.15 am to 12.30 pm

**Event : FACULTY DEVELOPMENT PROGRAM on
“DESIGN OF ELECTRICAL MACHINES”**

Venue : EEE Power System Simulation Lab

Prayer Song

Welcome Address : Ms.J.R.Bindhu
AP / EEE

Introduction to Guest : Mr.A.Ramaraj
AP / EEE

Felicitation Address

Dr.S.Sankaralingam, M.E, Ph.D,
Principal, SVCET, Virudhunagar.

Special Address

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Vote of Thanks: Mr.D.Pandiaraj
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